What is claimed is:

1. An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

detecting an attempted write operation to a protected area of a memory including a first set of instructions;

using a second set of instructions not located in the memory to determine that an authorization flag not located in the memory has been set by the first set of instructions; and

if the authorization flag has been set, enabling the attempted write operation.

2. The article of claim 1, wherein detecting an attempted write operation to the protected area includes:

detecting activation of at least two signal lines connected to the memory.

3. The article of claim 2, wherein detecting activation of the at least two signal lines connected to the memory includes:

simultaneously detecting activation of at least one address line connected to the memory and at least one access enabling line connected to the memory.

4. The article of claim 1, wherein detecting an attempted write operation to the protected area includes:

activating an interrupt line connected to a processor.

5. The article of claim 1, wherein the second set of instructions and the authorization flag are located in another memory.

6. The article of claim 1, wherein the second set of instructions is located in another memory, and wherein the authorization flag is not located in the other memory.

7. The article of claim 1, wherein using a second set of instructions not located in the memory to determine that an authorization flag not located in the memory has been set by the first set of instructions includes:

determining a value of a bit not located in the memory.

8. The article of claim 1, wherein enabling the attempted write operation includes:

activating at least one access enabling line connected to the memory.

9. The article of claim 8, wherein detecting an attempted write operation to the protected area includes:

simultaneously detecting activation of at least one address line connected to the memory and the at least one access enabling line connected to the memory.

10. The article of claim 1, wherein the data, when accessed, results in the machine performing:

detecting that the attempted write operation has been completed.

11. The article of claim 10, wherein detecting that the attempted write operation has been completed includes:

detecting an occurrence of a software interrupt.

12. The article of claim 10, wherein the data, when accessed, results in the machine performing:

disabling a future write operation to the protected area.

13. The article of claim 12, wherein disabling the future write operation to the protected area includes:

deactivating at least one access enabling line connected to the memory.

14. The article of claim 1, wherein the data, when accessed, results in the machine performing:

otherwise, if the authorization flag has not been set, refraining from enabling the attempted write operation.

15. An apparatus, comprising:

a first memory having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line;

a write detection module having an output coupled to an interrupt to indicate an attempt to write to the protected area; and

a second memory including a second set of instructions in operational communication with the interrupt, the second set of instructions adapted to determine the state of the flag.

16. The apparatus of claim 15, further comprising:

a third memory in operational communication with the second set of instructions, wherein the third memory includes the flag.

17. The apparatus of claim 15, wherein the write detection module and the second memory are included in a single integrated module.

18. The apparatus of claim 15, wherein the first memory comprises a flash memory.

19. An apparatus, comprising:

a network interface; and

a memory access control circuit operationally connected to the network interface, the memory access control circuit including a first memory having a protected area

including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line, a write detection module having an output coupled to an interrupt to indicate an attempt to write to the protected area, and a second memory including a second set of instructions in operational communication with the interrupt, the second set of instructions adapted to determine the state of the flag.

20. The apparatus of claim 19, wherein the access enabling line is operationally coupled to a processor.

21. The apparatus of claim 19, wherein the write detection module is included in a circuit.

22. The apparatus of claim 21, wherein the circuit is a processor.

23. A system, comprising:

a server; and

an apparatus capable of being coupled to the server, the apparatus including a first memory having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line, a write detection module having an output to indicate an attempt to write to the protected area, and a second memory including a second set of instructions in operational communication with the write detection module, the second set of instructions, upon execution, capable of determining the state of the flag.

24. The system of claim 23, wherein the apparatus is a set-top client.

25. The system of claim 23, wherein the server is coupled to the apparatus with a network.